REMARKS

By this Amendment, claims 1, 9 and 14 are amended, and claim 21 is added. Claims 5-8, 10-13 and 15-20 remain in the application. Thus, claims 1 and 5-21 are active in the application. Reexamination and reconsideration of the application are respectfully requested.

In item 1 on page 2 of the Office Action, claim 1 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. In particular, the Examiner asserted the limitation "plus-sizing" is vague and indefinite because it fails to set the metes and bounds of the claimed invention.

The Applicants submit that the term "plus-sizing" is clearly defined in lines 9-16 on page 5 of the substitute specification (lines 18-26 on page 5 of the original specification). Nevertheless, to clarify the invention of claim 1, the term "plus-sizing" has been removed from claim 1.

As described in lines 9-16 on page 5 and line 20 on page 7 to line 10 on page 8 of the substitute specification (lines 18-26 on page 5 and lines 8-26 on page 8 of the original specification), as well as in Figure 1(B), the dummy patterns of the present invention can be covered by depositing an insulating layer thereon even if the dummy pattern has spacing. This operation is referred to as "plus-sizing" in the present invention.

Claim 1 has been amended to recite that each of the plurality of dummy patterns has a plurality of line patters each of which is spaced apart with a width filled by the deposition of the insulating film.

The Applicants respectfully submit that claim 1, as amended, is clearly definite and particularly points out and distinctly claims the subject matter which the Applicants regard as the invention. Accordingly, the Applicants respectfully request withdrawal of the rejection of claim 1 under 35 U.S.C. § 112, second paragraph.

In item 2 on page 2 of the Office Action, claims 1 and 5-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Motoyama et al. (U.S. 6,099,992).

Without intending to acquiesce to this rejection, independent claims 1, 9 and 14 have been amended in order to more clearly illustrate the marked differences between the present invention and the applied reference. Accordingly, the Applicants respectfully

submit that the present application is clearly allowable over Motoyama et al. for the following reasons.

The present invention provides a semiconductor device having dummy patterns. The dummy patterns are formed in a pattern non-forming region or a non-pattern area within a same shape or having a same outline, as shown in Figures 1(A), 3(A), 4(A) and 5(A). In each shape or outline, a plurality of dummy line patterns (Figure 1(A)) or a single pattern with an opening (Figures 3(A), 4(A) and 5(A)) are formed.

As described in line 11 on page 2 to line 2 on page 3 of the substitute specification (line 13 on page 2 to line 5 on page 3 of the original specification), an insertion of dummy patterns reduces the global step so that a chemical mechanical polishing (CMP) of the insulating layer is thereby improved. However, an insertion of dummy patterns makes a pattern ratio large. Therefore, a disadvantage occurs with regard to an end detection of etching the pattern.

However, since each shape or outline of the dummy patterns of the present invention has a space portion (a space between the line patterns or the opening), a pattern ratio of the semiconductor device is reduced. Therefore, it is possible to more effectively suppress an increase in the global step that is formed by a deposition process (see, for example, lines 8-13 on page 9 of the substitute specification (lines 5-9 on page 10 of the original specification)).

Independent claims 1, 9 and 14 each recite the semiconductor device of the present invention as having the above-described features.

Claim 1 recites a semiconductor device which comprises a semiconductor substrate having a pattern forming region and a pattern non-forming region, and a wiring pattern formed on the pattern forming region. The semiconductor device of claim 1 also comprises a plurality of dummy patterns formed on the pattern non-forming region, where the plurality of dummy patters are formed within a plurality of dummy areas, and an insulating film formed on the wiring pattern and the plurality of dummy patterns. As defined in claim 1, the insulating film is formed by a chemical vapor deposition and is smoothed by chemical mechanical polishing (CMP). Furthermore, as also defined in claim 1, each of the plurality of dummy patterns has a plurality of line patterns each of which is spaced apart with a width filled by the deposition of the insulating film.

Claim 9 recites a semiconductor device which comprises a semiconductor substrate having a pattern area and a non-pattern area, and a conductive pattern formed on the pattern area of the semiconductor substrate. The semiconductor device of claim 9 also comprises a plurality of dummy patterns formed on the non-pattern area of the semiconductor substrate, where each of the plurality of dummy patterns has a same rectangular outline and is arranged in a matrix with predetermined spacing. The semiconductor device of claim 9 also comprises an insulating film formed on the wiring pattern and the plurality of dummy patterns. As defined in claim 9, the insulating film is formed by a chemical vapor deposition and is smoothed by chemical mechanical polishing. As also defined in claim 9, each of the plurality of dummy patterns has an opening so that a pattern ratio of the semiconductor device is reduced.

Claim 14 recites a semiconductor device which comprises a semiconductor substrate having a pattern area and a non-pattern area, a conductor pattern formed on the pattern area of the semiconductor substrate, and a plurality of dummy patterns formed on the non-pattern area of the semiconductor substrate. The semiconductor device of claim 14 also comprises an insulating film formed on the conductive pattern and the plurality of dummy patterns. As defined in claim 14, the insulating film is formed by a chemical vapor deposition and is smoothed by chemical mechanical polishing. As also defined in claim 14, each of the plurality of dummy patterns are formed in a plurality of dummy areas each having a same shape and being arranged in a matrix with predetermined spacing, and each of the plurality of dummy patterns has a space portion within each of the dummy areas so that a pattern ratio of the semiconductor device is reduced.

Motoyama et al. discloses a semiconductor device in which interconnection patterns 21 are laid on a substrate, and first dummy patterns 22 are disposed at a fixed interval W from the interconnection patterns 21 (see Column 7, lines 26-29 and Figure 5A). A lattice-like pattern 23 is then laid onto the first dummy patterns 22, and the portions of the first dummy patterns which are disposed under the lattice-like (reticular) pattern 23 are removed to form second (divided and separated) dummy patterns 22d-22h (see Column 7, lines 30-39 and Figures 5B-5C).

Accordingly, Motoyama et al. discloses a semiconductor device having dummy patterns. Motoyama et al. discloses that all of the areas including pattern areas and non-

pattern areas are divided in substantially the same shape or outline, as shown in Figure 5B. Motoyama et al. also discloses that a single dummy pattern without an opening is formed in each of the standard areas (dummy areas having the same shape), as shown in Figure 7A. For instance, Motoyama et al. discloses that in a top left dummy pattern (refer to arrows 1.65 in Figure 7A), there is a single dummy pattern in the whole area.

However, Motoyama et al. does not disclose or suggest that the insulating layer 36 and 37 is subjected to chemical mechanical polishing (CMP), and therefore, Motoyama et al. does not even contemplate a pattern ratio and reducing the global step. Accordingly, Motoyama et al. does not show a plurality of dummy line patterns or a single dummy pattern with an opening (space) for reducing a pattern ratio of the semiconductor device.

Therefore, Motoyama et al. clearly does not disclose or suggest a semiconductor device comprising an insulating film formed on the wiring pattern or conductive pattern and the plurality of dummy patterns, where the insulating film is formed by a chemical vapor deposition and is smoothed by chemical mechanical polishing, as recited in claims 1, 9 and 14.

Furthermore, Motoyama et al. clearly does not disclose or suggest that each of the plurality of dummy patterns has a plurality of line patterns each of which is spaced apart by the deposition of the insulating film, which is formed by a chemical vapor deposition and is smoothed by chemical mechanical polishing, as recited in claim 1.

Similarly, Motoyama et al. clearly does not disclose or suggest that each of the plurality of dummy patterns has an opening so that a pattern ratio of the semiconductor device is reduced, as recited in claim 9. Moreover, Motoyama et al. clearly does not disclose or suggest that each of the plurality of dummy patterns has a space portion within each of the dummy areas so that a pattern ratio of the semiconductor device is reduced, as recited in claim 14.

Accordingly, Motoyama et al. clearly does not disclose or suggest each and every limitation of claims 1, 9 and 14.

Therefore, claims 1, 9 and 14 are clearly not anticipated or rendered obvious by Motoyama et al. since Motoyama et al. fails to disclose each and every limitation of claims 1, 9 and 14. Furthermore, it is submitted that the clear distinctions discussed

above are such that a person having ordinary skill in the art at the time the invention was made would not have been motivated to modify

Accordingly, it is submitted that the claims 1, 9 and 14, as well as claims 5-8, 10-13 and 15-21 which depend therefrom, are clearly allowable over the prior art as applied by the Examiner.

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. An early notice thereof is respectfully solicited.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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